

# SLICE-OPL

## Offset Phase Lock Servo

The SLICE-OPL Offset Phase Lock Servo (OPLS) is designed to precisely control and quickly adjust the frequency detuning between a master and a follower laser. The SLICE-OPL forms a complete offset lock system when combined with the D2-250 Heterodyne Module and D2-260 Beat Note Detector. The D2-250 overlaps the free-space master & follower lasers to generate the optical beat note. It then launches the beat note into a fiber for delivery to the D2-260 where it is down-converted to the RF and then delivered to the SLICE-OPL for processing.

The SLICE-OPL is also designed for stabilizing frequency combs. With the ability to process beat notes as small as 10 MHz, the SLICE-OPL will tightly lock  $f_{\text{CEO}}$  and  $f_{\text{opt}}$  or  $f_{\text{rep}}$  of the FFC-100 series of frequency combs as well as 3rd-party combs.

The SLICE-OPL has a built in touch screen GUI with the ability to display and manipulate the error signal and engage the lock. No oscilloscope is required to initiate and monitor the lock.



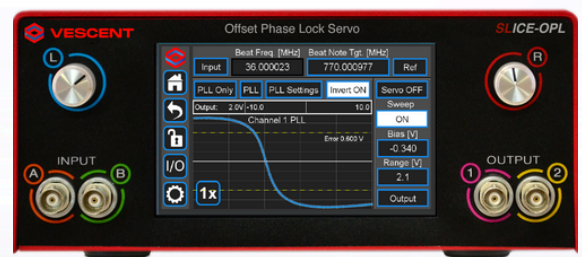
SLICE-OPL Offset Phase Lock Servo

### Features:

- Offset Phase Locks from 10 MHz to 9.3 GHz
- Touch screen GUI
- No oscilloscope required to operate!
- Precisely control follower laser frequency while remaining referenced to the primary standard
- Tightly lock  $f_{\text{CEO}}$  and  $f_{\text{opt}}$  or  $f_{\text{rep}}$  for frequency comb stabilization
- User-adjustable servo parameters
- Internal ramp generator
- Fast frequency jumps with feed-forward
- Offset frequency stability determined by reference stability

### Applications:

- Offset locking follower laser from master
- Frequency Comb stabilization



SLICE-OPL Touchscreen GUI

# SLICE-OPL & SLICE-DOPL Specifications

Parameter	Value
Number of Channels	1
Offset Range	10 MHz - 9.3 GHz
Loop Filter Transfer Function	PID
Operation Modes	Standby, Sweep, Proportional, PI, PID, LFGL, Integrator Hold
Control Bandwidth	>8 MHz
Internal Reference	DDS with software settable frequency
External Reference Input	Yes
External Reference Input Range to cover offset range	10 - 300 MHz
Proportional Gain	-30 dB to +40 dB
Prop Gain Resolution	$\leq 0.5$ dB
PI Corner Values (Hz)	100, 200, 500, 1k, 2k, 5k, ..., 1M, 2M, 5M
PD Corner Values (Hz)	150, 300, 600, ..., 1.5M, 3M, 6M
Low-Frequency Gain Limit	Yes
LFGL Range	$G_{prop} + 20$ to 80 dB
Integrator Hold	Yes
Internal Digital Ramp Range	$\pm 10$ V
Internal Digital Ramp Resolution	1/200 of Range
Internal Digital Ramp Rate	0.1 to 10 Hz
Internal Digital Ramp Output Port	Main Servo Out or Slow Servo Out
Output Voltage Clamp	Software Settable
Clamping Resolution	$\leq 100$ mV
Output Impedance	50 $\Omega$
Output Current Max	$\pm 30$ mA
Slow Servo Out (SSO)	Yes
SSO Transfer Function	Pure Integrator
SSO Modes	Enabled/Disabled
SSO Lock Point	User Settable
Power Input	100-230 VAC, 50-60 Hz